



PATENT  
P57002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Application of:

Appeal No. \_\_\_\_\_

TAE-SUNG KIM *et al.*

Serial No.: 10/767,281

Examiner: WARREN, MATTHEW E.

Filed: 30 January 2004

Art Unit: 2815

For: NOVEL CONDUCTIVE ELEMENTS FOR THIN FILM TRANSISTORS USED  
IN A FLAT PANEL DISPLAY

**SECOND SUBSTITUTE APPEAL BRIEF**

**Paper No. 29**

**Mail Stop Appeal Brief-Patents**

Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

Sir:

Pursuant to Appellants' Notice of Appeal filed on 11 June 2007, and the Office Communications of 27 August 2007 (Paper No. 20070824) and 10 January 2008 (Paper No. 20080104), Appellants hereby appeal to the Board of Patent Appeals and Interferences from the rejection of claims 1, 2, 4-9, 11-15, 17-19, and 21-24 as set forth in the fourth Office action mailed on 9 March 2007 (Paper No. 20070305).

Applicant previously filed an Appeal Brief on 22 November 2006 and the non-final Office action was issued on 9 March 2007 (Paper No. 20070305) in response to that Appeal Brief. Accordingly, no fee is incurred by filing of the instant Appeal Brief.

Folio: P57002

Date: 2/8/08

I.D.: REB/HMZ/kf



PATENT  
P57002

## TABLE OF CONTENTS

	<i>Page</i>
IDENTIFICATION .....	i
TABLE OF CONTENTS .....	ii
I. REAL PARTY IN INTEREST .....	1
II. RELATED APPEALS AND INTERFERENCES .....	2
III. STATUS OF CLAIMS .....	3
IV. STATUS OF AMENDMENTS .....	4
V. SUMMARY OF CLAIMED SUBJECT MATTER .....	5
VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL .....	8
VII. ARGUMENT .....	12
VIII. CLAIMS APPENDIX .....	16
IX. EVIDENCE APPENDIX .....	21
X. RELATED PROCEEDINGS APPENDIX .....	22



PATENT  
P57002

**I. REAL PARTY IN INTEREST**

Pursuant to 37 CFR §41.37(c)(1)(as amended), the real party in interest is:

SAMSUNG SDI CO., LTD.,  
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Republic of KOREA

as evidenced by the Assignment executed by the inventors on the 26<sup>th</sup> of January 2004 and recorded by the U.S. Patent and Trademark Office on the 30<sup>th</sup> of January 2004 at Reel 014944, Frame 0876.

## **II. RELATED APPEALS AND INTERFERENCES**

There are no other appeals and no interferences known to Appellant, Appellant's legal representatives or the assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

### **III. STATUS OF CLAIMS**

Claims 3, 10, 16, and 20 have been canceled. All remaining pending claims 1, 2, 4-9, 11-15, 17-19, and 21-24 are on appeal. Of all pending claims, claims 1, 8, 14 and 21 are independent, whereas the remaining claims are dependent.

#### **IV. STATUS OF AMENDMENTS**

An Amendment After Final was submitted to the U.S. Patent and Trademark Office on April 13, 2006. The Amendment After Final was entered as requested in the Request for Continued Examination (RCE) on May 15, 2006.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to four separate features as evidenced by the four independent claims and their respective dependent claims.

Namely, independent claim 1 and dependent claims 2 and 4-7 recite a thin film transistor. Independent claim 8 and dependent claims 9 and 11-13 recite a flat panel display. Independent claim 14 and dependent claims 15 and 17-19 recite a Thin Film Transistor (TFT). Lastly, independent claim 21 and dependent claims 22-24 recites a process for making a flat panel display.

With regard to independent claim 1 and dependent claims 2-7 (the thin film transistor), the specific features thereof are discussed in paragraphs [0042]-[0046] and illustrated in Figs. 2 and 7-10.

More particularly, Fig.10 illustrates a TFT including a source electrode 52, a drain electrode 53, and a gate electrode which is not shown in this drawing figure but which is connected to the gate channel 180. As noted in paragraph [0043], each of the source and drain electrodes includes an aluminum alloy layer 131 disposed between a pair of titanium layers 132 and 133 with a pair of diffusion prevention layers 138 and 139 disposed between the aluminum alloy layer and each of the pair of titanium layers. Paragraphs [0044]-[0046] specifically referred to the materials, the thicknesses, and alloy percentages of the layers illustrated in Fig.10 and recited in the claims dependent upon independent claim 1.

With regard to independent claim 8 and dependent claims 9 and 11-13 (the flat panel

display), the specific features thereof are discussed in paragraphs [0026]-[0039] and illustrated in Figs. 1-4.

More particularly, Fig. 3 illustrates a portion of a flat-panel display consisting of an electroluminescent display 114 while Fig.4 illustrates a portion of a flat-panel display consisting of a liquid crystal display 105. Furthermore, Fig.2 illustrates a driving unit of a flat-panel display provided with a first TFT 10 and a second TFT 50. Paragraphs [0028]-[0032] specifically discusses a first gate electrode 11, a first source electrode 12 and a first drain electrode 13 as well as a second source electrode 52, a second gate electrode 51 and a second drain electrode 53. In addition, paragraphs [0044]-[0046] specifically referred to the materials, the thicknesses, and alloy percentages of the layers illustrated in Fig.10 which corresponds to one of the TFTs 10 and 50 of Fig.2.

With regard to independent claim 14 and dependent claims 15 and 17-19 (the TFT), the specific features thereof are also discussed in paragraphs [0042]-[0046] and illustrated in Figs. 2 and 7-10.

More particularly, Fig.10 illustrates a TFT including a source electrode 52, a drain electrode 53, and a gate electrode which is not shown in this drawing figure but which is connected to the gate channel 180. As noted in paragraph [0043], each of the source and drain electrodes includes an aluminum alloy layer 131 disposed between a pair of titanium layers 132 and 133 with a pair of diffusion prevention layers 138 and 139 disposed between the aluminum alloy layer and each of the pair of titanium layers. Paragraphs [0044]-[0046] specifically referred to the materials,



the thicknesses, and alloy percentages of the layers illustrated in Fig.10 and recited in the claims dependent upon independent claim 14.

Lastly, with regard to independent claim 21 and dependent claims 22-24 (the process for making a flat panel display), the specific features thereof are discussed in paragraphs [0042]-[0051].

More particularly, claim 21 recites forming the specific elements recited in claim 8 and accordingly, Fig. 3 illustrates a portion of a flat-panel display consisting of an electroluminescent display 114 while Fig.4 illustrates a portion of a flat-panel display consisting of a liquid crystal display 105. Furthermore, Fig.2 illustrates a driving unit of a flat-panel display provided with a first TFT 10 and a second TFT 50. Paragraphs [0028]-[0032] specifically discusses a first gate electrode 11, a first source electrode 12 and a first drain electrode 13 as well as a second source electrode 52, a second gate electrode 51 and a second drain electrode 53. In addition, paragraphs [0044]-[0046] specifically referred to the materials, the thicknesses, and alloy percentages of the layers illustrated in Fig.10 which corresponds to one of the TFTs 10 and 50 of Fig.2.

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2, 4-7, 9, 14, 15, and 17-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ohtani *et al.* (U.S. Patent No. 6,271,543 B1) in view of Maeda (U.S. Patent No. 5,278,099)

In re claims 1 and 14, the Examiner states that Ohtani shows all of the elements of the claims except the aluminum layer being an aluminum alloy and a diffusion prevention layer interposed between the aluminum alloy layer and each of the pair of titanium layers. The Examiner states that Maeda shows the features deficient in Ohtani. The Examiner then argues that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the two references.

In re claims 2 and 15, the Examiner states that Maeda discloses (column 4, lines 22-31) that the aluminum alloy layer comprises an element selected from a group consisting of silicon, copper, neodymium, platinum and nickel. The Examiner then admits that Maeda does not disclose the specific weight percentage of the element in the alloy. The Examiner then argues that it would be obvious to combine references.

In re claim 4, the Examiner alleges that Maeda discloses (column 3, lines 46-61) each diffusion prevention layer is made of titanium nitride.

In re claims 5 and 6, the Examiner admits that the references do not teach the thickness of the titanium nitride or the percentage of nitrogen in the TiN being within the desired range.

However, it would have been obvious to one of ordinary skill in the art to make the thickness of the TiN layer or the percentage of nitrogen within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

In re claims 7 and 19, the Examiner states that Maeda discloses (column 4, lines 22-31) that the Al electrode is an alloy containing Si and is therefore absent of pure aluminum.

In re claims 17 and 18, the Examiner states that a “product by process” claim limitation is directed to the product per se, no matter how actually made. “Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process.” (Citation omitted).

In re the remaining limitations of claim 18 concerning the conductive channel formed between the source and drain electrodes, the Examiner alleges that Ohtani discloses (column 6, lines 63-67) that a channel is formed between the source and drain of the device. The semiconductor is also primarily made of silicon (column 6, lines 51-58) and contains the conductive channel.

Claims 8-13 and 21-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over

Ohtani *et al.* (U.S. Patent No. 6,271,543 B1) in view of Maeda (U.S. Patent No. 5,278,099) and Yamazaki *et al.* (U.S. Patent Publication No. 200310222575 A1).

In re claims 8 and 21, the Examiner alleges that Ohtani shows (Figures 2A-3A) a flat panel display and a process for making a flat panel display (column 6, line 38 - column 7, line 26) comprising forming: a substrate; a first plurality of thin film transistors formed on a surface of the substrate, the first plurality of thin film transistors comprising first source electrodes, first drain electrodes, first gate electrodes, and semiconductor layers; a plurality of first conductive lines electrically connected to the first source electrodes; and a plurality of second conductive lines electrically connected to the first gate electrodes. The Examiner then states that although Ohtani does not show the complete active matrix having a second plurality of thin film transistors, wherein the first drain electrodes of the first plurality of thin film transistors are electrically connected to gate electrodes of the second plurality of thin film transistors, such a recitation is of a well known routing scheme. For instance Yamazaki discloses [0175] a complete device having the gate electrode of one TFT connected to a drain electrode of another TFT for a driving circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the routing scheme of Ohtani by adding a plurality of TFTs and connecting them as taught by Yamazaki to form a complete device having a driving circuit.

Furthermore, the Examiner admits that Ohtani shows all of the elements of the claims except the alloy layer being an aluminum alloy and a diffusion prevention layer interposed between the aluminum alloy layer and each of the pair of titanium layers. The Examiner then argues that Maeda shows the features deficient in Ohtani and that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ti/Al/Ti source/drain

electrode of Ohtani by alloying Si with aluminum and forming TiN between the Ti and Al alloy layers as taught by Maeda to reduce resistance of the contact and prevent Al diffusion and the growth of alloy spikes.

In re claims 9 and 22, the Examiner states that Maeda discloses (column 4, lines 22-31) that the aluminum alloy layer comprises an element selected from a group consisting of silicon, copper, neodymium, platinum and nickel but does not disclose the specific weight percentage of the element in the alloy. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the aluminum alloy having the desired percentage of an element, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claims 11 and 23, the Examiner states that Maeda discloses (column 3, lines 46-61) each diffusion prevention layer is made of titanium nitride.

In re claims 12, 13, and 24, the Examiner admits that the references do not teach the thickness of the titanium nitride or the percentage of nitrogen in the TiN being within the desired range. However, it would have been obvious to one of ordinary skill in the art to make the thickness of the TiN layer or the percentage of nitrogen within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

## VII. ARGUMENT

The Examiner has correctly noted that Ohtani et al. teaches a three-layer laminated structure of titanium/aluminum/titanium for the source wiring line and drain electrode of Ohtani et al. (See lines 10-13 of column 7 of Ohtani et al.)

However, lines 59-62 of column 6 of Ohtani et al. indicate that a film of aluminum or a material mainly containing aluminum is formed and patterned to form the gate wiring line of Ohtani et al.

Accordingly, it is submitted that Ohtani et al. teaches away from a three-layer laminated structure of titanium/aluminum alloy/titanium in that there is an inference that Ohtani's failure to indicate that an aluminum alloy can be used for the source wiring line and drain electrode after previously indicating that an aluminum or aluminum alloy can be used for the gate wiring line infers that Ohtani only considered pure aluminum for the source wiring line and drain electrode.

Furthermore, while Maeda indicates in lines 22-31 of column 4 thereof that the layer 36 is not limited to pure aluminum but rather can be an aluminum alloy, Maeda indicates in lines 62-64 of column 3 thereof that since the TiN layer 34 has a thickness sufficient to prevent the growth of alloy spikes, aluminum layer 36 need not contain silicon. Accordingly, there is an inference that the use of a TiN layer precludes the need for an aluminum alloy layer and allows the layer 36 to be pure aluminum.

The independent claims recite that one of the source electrode and drain electrode

comprises an aluminum alloy layer disposed between a pair of titanium layers. That is, the recitation that the gate electrode comprises an aluminum alloy layer disposed between a pair of titanium layers has been deleted.

Ohtani et al., on the other hand, refers to a titanium/aluminum/titanium structure only for the source and drain electrodes and refers to an aluminum alloy only for the gate electrodes. Thus, the source and drain electrodes of Ohtani et al. do not correspond to the recited source and drain electrodes of the independent claims.

In responding to the above-noted arguments contained in the previously submitted September 27, 2005 Amendment and April 13, 2006 Amendment After Final, the Examiner **admits** on page 7 of the July 28, 2006 Office Action that “Ohtani . . . does not specifically disclose that the Al layer is an aluminum alloy layer.” The Examiner then continues: “The gate electrode having the same Ti/Al/Ti structure is cited in Ohtani as using an Al layer. Therefore, it is **assumed** that the source and drain electrodes of Ohtani **may** also comprise an Al alloy.” (Emphasis added)

Appellants strongly disagree with the Examiner’s unsupported assumptions. That is, there is no teaching or suggestion or incentive in Ohtani to fabricate the source and drain electrodes with the same material used to fabricate the gate electrode. In fact, the source and drain electrodes are oftentimes of a different material than that used for the gate electrode.

Furthermore, even assuming arguendo that the source and drain electrodes are of the same material as the gate electrode, this does not result in the conclusion that it would be obvious to

fabricate the source and drain electrodes of the same material as the gate electrode.

Stated simply, it is settled patent law that merely because one can modify a subject device in a reference to produce a device which purportedly meets the recited limitations of a rejected claim does not mean that it would be obvious to do so. The Examiner has used the wrong criterion to argue the obviousness of modifying a reference.

Furthermore, the Examiner argues that Maeda was cited to cure the deficiencies of Ohtani in that Maeda discloses that an electrode can comprise an alloy of aluminum. Again, the Examiner has used the wrong criterion to argue the obviousness of modifying a reference.

As to the recited specific weight percentage of the element in the alloy and the thickness of the titanium nitride layer or the percentage of nitrogen within the desired range, the Examiner has made an unsupported statement that these recited features would be obvious to one skilled in the art. Yet, the Examiner admits that neither Ohtani nor Maeda teaches or suggests these recited features, nor has the Examiner submitted secondary references which teach or suggest these recited features.

As to the rejection of claim 18, even disregarding the recited process limitation, claim 18 recites that the semiconductor of layer forming a conductive channel between the source electrode and drain electrode upon application of a voltage to the gate electrode does not appear to have been considered by the Examiner.

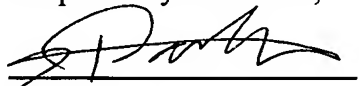


With regard to the specific comments by the Examiner in rejecting claims 8 and 21, the Examiner admits that Ohtani does not show the complete active-matrix having a second plurality of thin-film transistors, wherein the first drain electrodes of the first plurality of thin-film transistors are electrically connected to gate electrodes of the second plurality of thin-film transistors. The Examiner then argues that such a recitation is that of a well-known routing scheme and then cites the Yamazaki publication as teaching such a feature.

However, the Examiner has only rejected claims 8 and 21 as obvious over the combination of Ohtani and Maeda and the inclusion of the citation of the Yamazaki publication is therefore improper.

In conclusion, it is submitted that it would not be obvious to combine the features of Ohtani and Maeda in the fashion noted by the Examiner such that it is submitted that all of the claims now on appeal are patentable over the combination of Ohtani and Maeda and should now be in a condition suitable for allowance.

Respectfully submitted,

  
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## VIII. APPENDIX

### CLAIMS UNDER APPEAL (Claims 1, 2, 4-9, 11-15, 17-19, 21-24)

1           1. (Previously Presented) A thin film transistor, comprising a source electrode, a drain  
2           electrode, a gate electrode and a semiconductor layer, wherein one of the source electrode and  
3           drain electrode comprises an aluminum alloy layer disposed between a pair of titanium layers,  
4           wherein a diffusion prevention layer is interposed between the aluminum alloy layer and each of  
5           the pair of titanium layers, and wherein the aluminum alloy layer comprises at least one element  
6           selected from a group consisting of silicon, copper, neodymium, platinum and nickel.

1           2. (Original) The thin film transistor of claim 1, wherein the aluminum alloy layer  
2           comprises about 0.1 to 5 wt% of at least one element selected from a group consisting of silicon,  
3           copper, neodymium, platinum and nickel.

1           4. (Previously Presented) The thin film transistor of claim 1, wherein each diffusion  
2           prevention layer is made of titanium nitride.

1           5. (Previously Presented) The thin film transistor of claim 4, wherein each titanium nitride  
2           layer has a thickness between 100 and 500Å.

1           6. (Previously Presented) The thin film transistor of claim 4, wherein each titanium nitride  
2           layer contains 5 to 85 wt% of nitrogen.

1           7. (Original) The thin film transistor of claim 1, each electrode being absent of pure

aluminum.

8. (Previously Presented) A flat panel display, comprising:

a substrate;

a first plurality of thin film transistors formed on a surface of the substrate, the first plurality of thin film transistors comprising first source electrodes, first drain electrodes, first gate electrodes, and semiconductor layers;

a plurality of first conductive lines electrically connected to the first source electrodes; and

a plurality of second conductive lines electrically connected to the first gate electrodes;

a second plurality of thin film transistors, wherein the first drain electrodes of the first plurality of thin film transistors are electrically connected to gate electrodes of the second plurality of thin film transistors, wherein one of the first source electrodes, the first drain electrodes, the plurality of first conductive lines, and the plurality of second conductive lines comprises an aluminum alloy layer and a titanium layer formed on both surfaces of the aluminum alloy layer, wherein a diffusion prevention layer is interposed between the aluminum alloy layer and the titanium layers, and wherein the aluminum alloy layer comprises at least one element selected from a group consisting of silicon, copper, neodymium, platinum and nickel.

9. (Original) The flat panel display of claim 8, wherein the aluminum alloy layer comprises about 0.1 to 5 wt% of at least one element selected from the group consisting of silicon, copper, neodymium, platinum and nickel.

11. (Previously Presented) The flat panel display of claim 8, wherein each diffusion prevention layer is made of titanium nitride.

1           12. (Previously Presented) The flat panel display of claim 11, wherein each titanium nitride  
2 layer has a thickness between 100 to 500Å.

1           13. (Original) The flat panel display of claim 11, wherein each titanium nitride layer  
2 contains 5 to 85 wt% of nitrogen.

1           14. (Previously Presented) A TFT, comprising:  
2 a source electrode, a gate electrode and a drain electrode; and  
3 a semiconductor layer between the source electrode and the drain electrode, wherein one  
4 of said source electrode and said drain electrode contain an aluminum alloy layer bounded by a  
5 pair of titanium layers and not a pure aluminum layer, wherein said source electrode and said drain  
6 electrode each comprising a TiN diffusion prevention layer between the aluminum alloy layer and  
7 each titanium layer, and wherein the aluminum alloy layer comprises at least one element selected  
8 from a group consisting of silicon, copper, neodymium, platinum and nickel.

9           15. (Original) The TFT of claim 14, wherein the aluminum alloy layer comprises about 0.1  
10 to 5 wt% of at least one element selected from the group consisting of silicon, copper, neodymium,  
11 platinum and nickel.

1           17. (Original) The TFT of claim 14, said semiconductor layer being absent of aluminum  
2 after said TFT is subjected to a heat treatment of at least 300 degrees Celsius.

1           18. (Original) The TFT of claim 14, said semiconductor layer being primarily made of  
2           silicon and said semiconductive layer forming a conductive channel between said source electrode  
3           and said drain electrode upon application of a voltage to the gate electrode after said TFT is  
4           exposed to heat of at least 300 degrees Celsius.

1           19. (Original) The TFT of claim 14, said source electrode and said drain electrode both  
2           being formed of aluminum alloy and both being absent pure aluminum.

1           21. (Previously Presented) A process for making a flat panel display, comprising:  
2           forming a first plurality of thin film transistors formed on a surface of a substrate, the first  
3           plurality of thin film transistors comprising first source electrodes, first drain electrodes, first gate  
4           electrodes, and semiconductor layers;

5           electrically connecting a plurality of first conductive lines to the first source electrodes;

6           electrically connecting a plurality of second conductive lines to the first gate electrodes;

7           and

8           forming a second plurality of thin film transistors, electrically connecting the first drain  
9           electrodes of the first plurality of thin film transistors to gate electrodes of the second plurality of  
10          thin film transistors, wherein one of the first source electrodes, the first drain electrodes, the  
11          plurality of first conductive lines, and the plurality of second conductive lines comprises an  
12          aluminum alloy layer and a titanium layer formed on both surfaces of the aluminum alloy layer,  
13          and interposing a diffusion prevention layer between the aluminum alloy layer and the titanium  
14          layers, and wherein the aluminum alloy layer comprises at least one element selected from a group  
15          consisting of silicon, copper, neodymium, platinum and nickel.

1           22. (Previously Presented) The process of claim 21, comprised of making the aluminum  
2 alloy layer from an aluminum alloy comprising about 0.1 to 5 wt% of at least one element selected  
3 from the group consisting of silicon, copper, neodymium, platinum and nickel.

1           23. (Previously Presented) The process of claim 21, comprised of making the diffusion  
2 prevention layers of titanium nitride.

1           24. (Previously Presented) The process of claim 23, comprised of making the titanium  
2 nitride layers with a thickness between 100 to 500Å.

**IX. EVIDENCE APPENDIX**

None.

**X. RELATED PROCEEDINGS APPENDIX**

None.